Technology – NAND Flash Memory Chips Are Used in Thumbdrives, Flash Memory Cards and MP3 Players

Flash Memory Chip Technology

In current designs of flash memory chips, there is a thin layer of silicon dioxide that coats the transistor gates of flash chips which allows the flash memory chips to retain memory even when power is cut off. This silicon layer holds electrons within the transistor gate. Depending on the nature of the electrons' charge, the device using the flash memory reads the charge as "on" or "off," creating the ones and zeroes necessary for binary information.

This silicon dioxide layer has been reduced down in size continually as flash memory's production process has progressed over time. For flash memory manufacturers, this shrinkage is essential to increasing profits. A smaller chip allows fabricators to make more chips from a single wafer. It also allows a greater size-to-performance ratio.

But scientists say silicon dioxide is reaching its limits. At the current pace of innovation in the production process, the material will have been scaled down as far as possible within the next two years.

The Flash Memory Chip of the Future

One of the first things experts like to point out about flash is that, technically, it's contradictory. Flash chips are electrical, meaning that they need electricity to store data. Yet flash chips retain their data after the host computer or cell phone is turned off.

The trick lies in the fact that the gate in a flash transistor--the microscopic on-off switch inside a flash chip--is wrapped in a layer of silicon dioxide that prevents electrons from escaping. Depending on what the charge inside is, the computer reads the memory cell as a "1" or "0".

The silicon dioxide insulator is so effective that a floating gate transistor (so-called because the gate "floats" above the rest of the transistor) will retain data for 10 years. New data can be written to a flash chip a million times before errors begin to occur. While the insulating layer is the secret layer in the flash design, it also is the source of problems. The silicon dioxide wrappers on flash chips today measure about 90 angstroms thick. An angstrom is one ten-billionth of a meter, or less than the width of a hydrogen atom and can probably be reduced in size to about 80 angstroms. Any thinner, and the electrons begin to leak out, leading to data corruption or loss.

In its turn, the need for thickness makes power a problem. About 10 volts must be applied to the floating gate to get electrons through in the first place and far more voltage than is used to animate microprocessor transistors.

In addition, if the size of the chip is reduced, the voltage intended for one cell might inadvertently zap a neighboring cell which results in misrecorded data.

Consequently, as existing technology nears its limits, manufacturers are eager to develop new designs. For example, Texas Instruments and Ramtron both have worked with ferroelectric RAM (FeRAM), which uses moving atoms within a crystal. And Intel is testing Ovionics Unified Memory, in which data is retained in a heated material similar to that used in DVD discs. Motorola is working with crystal materials in their research and development.

To increase capacity and to makel flash chips with an average component size of 45 nanometers in the future is the goal for the flash memory chip manufacturing process which is set begin in 2007.

NAND Flash

NAND Flash Memory Chips are the type used in thumbdrives, flash memory cards and MP3 Players. NAND flash memory chips are built into these USB memory products on which consumers store images, video and music. These products are all available with Gigabyte capacity.

Eight bits of memory chip power are required to run one byte of storage capacity, which is enough to store a single letter of the alphabet. Eight Bits make one Byte and the chart below provides the Gigabit and Megabit chip capacities required to make Gigabyte Capacities on thumbdrives and FlashPoint ShareDrives.

Flash Memory Capacity Composition of USB Flash Memory Drive

USB Thum Drive Capacity	**Flash Memory Chip Used**
2 GB	8G (1G*8) chip * 2 pcs
1 GB	8 GB (1GB*8) chip* 1 pcs or 4 GB (512MB*8) chip* 2 pcs
512 MB	512 MB 4G (512MB*8) Chip *1 pcs or 2G (256MB*8) Chip*2 pcs
256 MB	2G (256MB*8) chip* 1 pcs or 1G (128MB*8) * 2 pcs
128 MB	1G (128MB*8) * 1

NAND flash was developed for its reduced cost and size. Its design emphasizes increased write performance, higher density, and lower cost. Write performance improvements are achieved through a sector-oriented management of the flash and smaller sized erase blocks. Higher densities are attained by using a smaller flash cell size. The scaled back cell size, and the reduced pin count of NAND's I/O interface, contribute to a lower manufacturing cost.

On host systems, NAND is readily connected via the same simple interface commonly found in many computer peripherals. Instead of requiring full data and address bus lines, data and commands are multiplexed onto eight I/O lines. This consumes only three addresses in the host's I/O space. Using this conduit into the flash, a register set can be read and written to dispatch commands and access data. Each time a read or write command is issued, the amount of data transferred is always one page consisting of 528 bytes (512 bytes of data and 16 bytes typically containing ECC). This is the marked distinction between the NAND and NOR interfaces: data transfers with NAND flash always involve the issuing of a command and the accessing of a page's worth of data. There is no ability to randomly access a few selected bytes, and it's not possible to linearly address the flash, thus directly executing code from NAND is out of the question: SDRAM shadowing must always be employed for code storage applications. With NAND, data from each page is always transferred one byte at a time.

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